REMARKS

Claims 1-5, 7-20, 23-33 and 55 are pending in this application. Applicants gratefully acknowledge allowance of claims 1-5, 7-20, 23-27 and 55.

Claim 28 stands rejected under 35 U.S.C. § 103 (a) as being obvious in view of U.S. Patent 5,329,142 to Kitagawa et al. ("Kitagawa et al.") in combination with U.S. Application 2004/0062110 to Shirley ("Shirley"). Claims 29-33 stand objected to as depending from a rejected base claim. The rejection and objection are respectfully traversed.

Claim 28 defines a computer system, including a memory circuit connected to a processor and recites "two gated complementary bipolar transistors and having bistable current states for storing information, one of said current states being achieved by operation of gate-induced latch-up of said transistors, wherein the complementary bipolar transistors comprise a vertical p-n-p transistor and a vertical n-p-n transistor and the collector region of said p-n-p transistor is connected with the base region of said n-p-n transistor." Neither Kitagawa et al. nor Shirley, taken individually or in combination, teach or suggest a device as claimed.

Kitagawa et al. does not teach or suggest a device "having bistable current states for storing information," as recited in the claim. It is not taught or suggested by Kitagawa et al. that its disclosed device can even store information. Furthermore, as noted in the Office Action at page 2, Kitagawa et al. fails to teach a processor connected to the memory circuit.

Additionally, Kitagawa et al. teaches away from the claimed device, thereby, Kitagawa et al. is an improper reference for a rejection under 35 U.S.C. § 103(a). Kitagawa et al. instructs that its transistors are configured to prevent the device "from

being latched up." Column 5, line 68; column 6, lines 19-25; column 9, lines 57-58; and column 21, lines 43-44, 61-62. Thus, it is apparent that Kitagawa et al. directly teaches away from the recited "operation of gate-induced latch-up of said transistors" of claim 28. For this reason alone, the rejection of claim 28 should be withdrawn.

Furthermore, the disclosure of Shirley cannot make up for the inadequacies of the Kitagawa et al. disclosure. Particularly, Shirley does not disclose "two gated complementary bipolar transistors and having bistable current states for storing information, one of said current states being achieved by operation of gate-induced latch-up of said transistors" as recited by claim 28. Therefore, neither Kitagawa et al. nor Shirley, taken individually or in combination, teach or suggest all of the limitations recited in independent claim 28. Accordingly, Applicants respectfully request withdrawal of the rejection under 35 U.S.C. §103 (a).

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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